Sub H2

83. (New) The method of claim 80, further comprising:

subsequently switching from the pipelined mode of operation to the burst mode of operation;

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on February 1, 2001, and the references cited therewith. The Applicant's representative has reviewed the other art made of record by the Office, but believes that the cited references are more pertinent to the instant application. No claims have been amended, claims 70-74 are canceled, and claims 75-83 are added; as a result, claims 36-39, 59-69, and 75-83 are now pending in this application.

Restriction Requirement

Claims 70- 74 were withdrawn from further consideration by the Examiner as being drawn to a non-elected invention. The Applicant elects to continue prosecution, without traverse, with claims 36-39, 59-69, as well as with new claims 75-83. The Applicant respectfully cancels claims 70-74 without prejudice, and reserves the right to reintroduce them in a divisional application at a later date.

Double Patenting Rejection

In §5 of the Office Action, claim 66 was provisionally rejected under the judicially created doctrine of double patenting over claims 51, 59, 63, 64, and 67 of co-pending Application No. 08/984.561, which has not yet received any final indication of allowed claims. The Applicant requests that the claims of the instant patent application be allowed to issue without a Terminal Disclaimer, and that the issued claims of the instant application be compared to the claims of the cited co-pending application to determine if a judicially-created non-statutory double patenting rejection is required. If so, the Applicant will submit a Terminal Disclaimer to obviate any remaining double patenting rejection upon closing prosecution on the merits for the

co-pending application, as needed, or in the alternative, upon receiving an indication of allowance for the relevant claims in the instant application.

Claim Objections

In §6 of the Office Action, claims 70 and 74 were objected to because of informalities. However, claims 70-74 have been canceled. Thus, the Applicant respectfully notes that the rejection is now moot.

In §7 of the Office Action, claims 36, 68, and 69 were objected to under 37 C.F.R. 1.75(b) as not substantially differing from each other. The Applicant respectfully submits that claims 36, 68, and 69 are clearly different from each other. In particular, claim 36 recites the step of "receiving an external row address", and claim 68 recites the steps of "obtaining an initial external column address ... and generating internal column addresses". Claim 69, being a claim to a storage device, recites no method steps; instead, claim 69 recites a device including elements not recited by claims 36 or 68. Neither of these steps or elements is the same as the other; each has a clearly defined difference according to the recited elements. Clearly, the requirement of receiving an external row address is absent from claims 68 and 69. Moreover, the elements recited in claim 69 are missing from claims 36 and 68. Thus, withdrawal of this objection is respectfully requested.

§112 Rejection of the Claims

Claims 73 and 74 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. However, claims 70-74 have been canceled. Thus, the Applicant respectfully notes that the rejection is now moot.

§102 Rejection of the Claims

Claims 36-39 and 59-62 were rejected under 35 USC § 102(e) as being anticipated by Manning (U.S. Patent No. 5,610,864). The MPEP requires that "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131. Thus, the

Applicant asserts that the Office has failed to show that Manning discusses the identical invention claimed in the instant application, and respectfully traverses the rejection by the Office.

The Office has failed to produce a *prima facie* case of anticipation. For example, the Applicant cannot find, and the Office has failed to show, where Manning discusses the ability to choose, select, or switch between burst and pipelined *modes* of operation. The Office asserts that Manning discusses a pipelined mode of operation, when the actual text of Manning refers to a "pipelined architecture" as being applicable to Manning's invention (*See* Manning at column 5, lines 43-50). Does Manning refer to individually addressing and accessing memory data in a pipelined fashion, as defined by the Applicant, or merely driving data outputs in a pipelined fashion while operating in a burst mode? According to Manning, a pipelined architecture is "where memory accesses are performed sequentially, but each access requires more than one cycle to complete." This definition doesn't appear to markedly differentiate pipelined memory access from burst operations. Thus, Manning merely discloses the possibility that a pipelined *architecture* (as opposed to a mode of operation) might be "applicable to the current invention" (without disclosing how such an application might occur). While Manning does specifically discuss the option of "switching between burst EDO and standard EDO modes of operation" (See Manning at col. 6, lines 14-16), Manning never extends this idea to switching between a pipelined *mode of operation*, and a burst mode of operation. Thus, the assertion by the Office that "Manning discloses a method of accessing a memory comprising ... choosing whether the memory is in burst or a pipelined mode of oepration", or "... switching between a burst mode and a pipeline mode", or "selecting between a burst and a pipelined mode of operation" is simply not supported using any of the teachings of Manning. Thus, the Applicant cannot find, and the Office has failed to show, a single instance where Manning discusses switching memory access activity between burst and pipelined *modes of operation*, as claimed by the Applicant in independent claims 36 and 59, and the claims which depend from them.

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the M.P.E.P., and therefore, the rejection is improper. Reconsideration and allowance of claims 36-39 and 59-62 is therefore respectfully requested.

§103 Rejection of the Claims

Claims 63-69 were rejected under 35 USC § 103(a) as being unpatentable over Manning (U.S. Patent No. 5,610,864) in view of Ryan (U.S. Patent No. 5,966,724) or Rosich et al. (U.S. Patent No. 5,587,964). The Applicant respectfully traverses this rejection by the Office.

The Applicant is unable to find, and the Office has failed to show, how Ryan or Rosich et al., in combination with each other, or with Manning, serve to teach the invention disclosed in claims 63-69. The Applicant has previously discussed why Manning is defective as a reference (i.e., Manning fails to disclose switching between burst and pipelined modes of operation). Ryan and Rosich et al. also fail to teach *switching* between burst and pipelined modes of operation. Ryan teaches standard EDO, fast page mode EDO, and burst EDO modes of operation, without any teaching of how one might switch to a pipelined access mode. Rosich et al. merely discloses switching between a page mode and a nibble mode. There is no discussion of a pipelined access mode by Rosich et al., whatsoever. Thus, the combination of Ryan and/or Rosich et al. with Manning does not cure the primary defect of Manning.

Further, Ryan teaches a synchronous memory device. *See* the Title and the Abstract of Ryan. As the Office notes, Manning discusses an asynchronous memory device. *See* for example, page 3 of the Office Action dated April 25, 2000. One of ordinary skill in the art would not be led to combine the dissimilar operation of these two devices. Further the M.P.E.P. requires that the asserted combination of the references must not change the principle of operation of the reference being modified. *See* M.P.E.P. § 2143.01. In this case, imposing synchronous operations on an asynchronous memory clearly changes the fundamental principle of operation for the asynchronous device. Therefore, the Applicant respectfully submits that combining Manning and Ryan would be improper.

Claims 70-74 were rejected under 35 USC § 103(a) as being unpatentable over Manning (U.S. Patent No. 5,610,864) in view of Micron 1996 DRAM Data Book (pp. 1-3). Claims 70-74 have been canceled. Thus, the Applicant respectfully notes that the objection to claims 70-74 is moot.

New Claims

Claims 75-83 have been added. It is noted that each of claims 75-83 incorporate all of the elements of claim 36. Thus, consideration and entry of claims 75-83 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6913 to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JEFFREY S. MAILLOUX ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 5/1/2001 By Edward J. Brooks III

Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this _____ day of May, 2001.

Name _______________ Signature _______________